Application Note

HCSL Reference Clocks

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High Speed Current Steering Logic

High Speed Current Steering Logic [HCSL] outputs are found in Peripheral Component Interconnect Express [PCIe] applications, Intel and Nvidia chipsets among others. HCSL is a differential output standard, similar to LVPECL, providing a high impedance output with fast switching times. Other advantages include average power consumption when compared to LVDS and LVPECL and low phase jitter performance.

The differential output has a 15mA current source derived from an open emitter or source, with unterminated drains, that require external 50 ohm resistors terminated to ground. If needed, a 10 to 30 ohm series resistor can be added to reduce overshoot or ringing in waveform. See Figures 1 and 2.

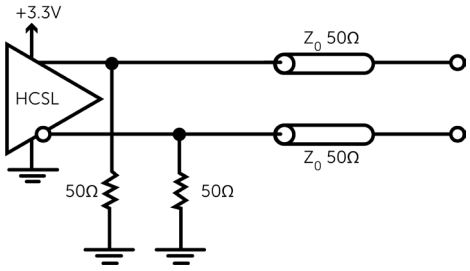

Figure 1: External Resistors [50 ohm] Terminated to Ground

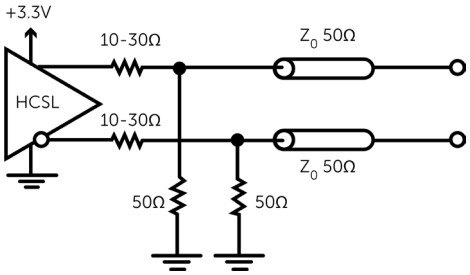

Figure 2: Series Resistors [10 – 30 ohm] Added to Reduce Overshoot

Peripheral Component Interconnect Express [PCIe]

PCIe is a serial point-to-point interconnect standard developed by the PCI Special Interest Group [PCI SIG], originally for the PC market to help computer manufacturers implement the Intel specification. However, due to its low cost and high data throughput, PCIe has been adopted in several application standards including blade servers, data storage [SATAe & M.2], embedded computing, 3D graphics, networking [Gigabit Ethernet], and communication platforms. In view of its popularity, simplicity and scalability; the PCIe electrical interface is being used in ASICs, FPGAs and SoCs. This provides designers with flexible solutions for high speed data transfer in their systems.

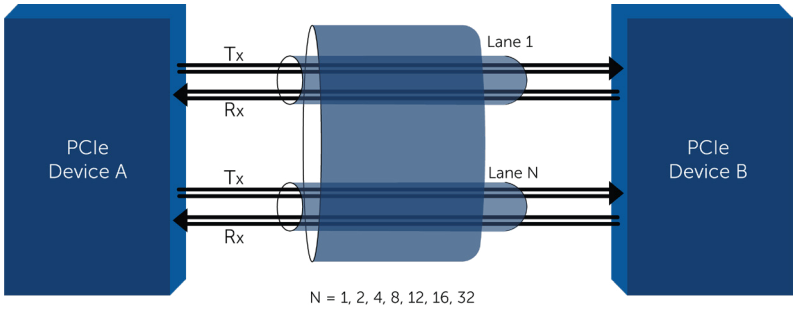

Figure 3: PCIe Data Link

PCIe Link Width	x1	x2	x4	x8	x12	x16	x32
Aggregate Bandwidth [Gbps]	0.5	1	2	4	6	8	16

Figure 4: PCIe Data Transfer Rates

The basic PCIe architecture consists of a data link between two devices that can have 1 to 32 lanes. The lanes are differentiated as x1, x2, x4, x8, x12, x16 and x32 PCIe links. Each lane is defined by differential pair of wires, one pair for transmitting [Tx] and the other pair for receiving [Rx] data. A single lane will carry data at a rate of 1 bit per cycle, therefore adding more lanes will increase the transfer rate. See figures 3 and 4.

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PCI Express Clock Requirements

An external reference clock is required to transmit the data. The standard clock requirements include a frequency of 100MHz, stability ±300ppm maximum and HCSL output. Although the reference clock frequency has remained the same for all PCIe generations, from PCIe1.0 to PCIe4.0, the jitter requirements have improved to support the higher transfer rates in succeeding versions. A history of PCIe clock jitter requirements are outlined in table Table 1, as well as highlighting the new Gen5.0 standard that is developing in 2019.

Jitter of the reference clock has a direct impact on the efficiency of the data transfer between devices. The improvement in jitter performance help eliminate delays in data transfer and give flexibility to the designer.

Note: In some FPGA applications that support both PCIe and Ethernet functions, a reference clock with other frequencies and output types maybe used; 125MHz, 200MHz or 250MHz in LVCMOS, LVDS or LVPECL. The FPGA will internally multiply the frequency to the required PCIe lane rate, i.e. 125MHz x64 for PCIe3.0. CTS has low jitter clock solutions for these options as well

PCIe Generation	Transfer Rate [GBPS]	Common Clock Jitter Limit [@ Receiver Latch]
1.0	2.5	108ps pk - pk
2.0	5	3.1ps$_{RMS}$
3.0	8	1.0ps$_{RMS}$
4.0	16	500fs$_{RMS}$
5.0	30	150fs$_{RMS}$

Table 1

CTS HCSL Clock Reference

A customer has two options to generate the clock signal required for PCIe data transferring.
1] A 100MHz HCSL output clock oscillator and a buffer that generates multiple clock signals.
2] A 25MHz crystal and a PLL that multiples the reference to generate the 100MHz clock signal.

The CTS solution provides a low jitter clock oscillator needed for Item 1 above.

Product Summary

CTS Clock Parameters	Advantages
Models 643H, 645H, and 647H	Multiple package sizes w/ industry standard pinout for drop-in replacement
100MHz Typical Frequency	Standard Disty stock for off-the-shelf availability
HCSL Output	Waveform parameters providing high speed switching
RMS Jitter [12kHz -20MHz], <500fs	Provides more design margin to ensure robust system performance
Operating Temperature Range -40°C/+105°C	Supporting extended temperature applications
Custom Frequencies Available	Application design flexibility
Voltage Options, 2.5V & 3.3V	
Frequency Stability Options, ±25ppm, ±30ppm, ±50ppm	
Output Enable [OE] standard	

Common PCI Express Markets

Enterprise Computing	Communications	Consumer/ Embedded
Network Servers Workstation Data storage Data Center SSD Memory Cloud Computing	Ethernet Cards Routers Access Points Switches Hubs Small Networks	Digital TV Set Top Box Printer Audio/Video Gateways Gaming

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Conclusion

The PCIe standard is a core technology used to interconnect peripheral devices in several application standards. With the development of PCIe 5.0, it will enable the mass adoption of the 400GE technologies, due to its full-duplex bandwith of approximately 128GB/s for a 16-lane system. This will become key for next-generation technologies needed to support the response times and high bandwith requirements of 5G and IoT.

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Clock Models		Features	Package Size [mm]	Output Logic	Frequency Range [MHz]	Temperature Stability [ppm]	Temperature Range [°C]	Supply Voltage [V]	Phase Jitter [fstyp]
General Products	643H	6-pad	3.2x2.5	HCSL	13.5 – 156.25	±25, ±30, ±50	-20 to +70 -40 to +85	2.5, 3.3	500
	645H	6-pad	5.0x3.2	HCSL	13.5 – 156.25	±25, ±30, ±50	-20 to +70 -40 to +85	2.5, 3.3	500
	647H	6-pad	7.0x5.0	HCSL	13.5 – 156.25	±25, ±30, ±50	-20 to +70 -40 to +85	2.5, 3.3	500

Applications

PCI Express [PCIe]
Data Storage Systems
Ethernet Line Cards
Serial ATA Express [SATAe]
Intel and Nvidia Chipsets
Network Servers
Switches and Routers
Set-Top Boxes/DVRs

Features

HCSL Output Logic
Low Phase Jitter
100MHz Common Frequency