Model CC Series

Advanced PLL LVPECL or LVDS Clock

Part Dimensions:
3.2 × 2.5 × 1.2mm • 26.64mg
5.0 × 3.2 × 1.5mm • 61.8mg
7.0 × 5.0 × 1.9mm • 172.74mg

Features

- Ceramic Surface Mount Package
- Very Low Phase Jitter Performance, 150fs Typical
- Quartz Crystal Based Design
- Frequency Range to 2.1GHz *
- +1.8V, +2.5V or +3.3V Operation
- Output Enable Standard
- Tape and Reel Packaging, EIA-481

Applications

- SerDes
- Storage Area Networking
- Broadband Access
- SONET/SDH/DWDM
- PON
- Ethernet/Gbe/SyncE
- Fiber Channel
- Medical Electronics
- Test and Measurement

Description

CTS Model CC Series is a high-performance clock oscillator supporting differential LVPECL or LVDS outputs. Employing the latest IC technology, CC Series has excellent stability and low jitter/phase noise performance.

Ordering Information

Model	Package Size	Output Type	Frequency Stability	Temperature Range	Supply Voltage	Frequency Code (MHz)	Packaging
CC	3	P	3	I	L	1244M16000	R

Code	Dimensions
3	3.2mmx2.5mm
5	5.0mmx3.2mm
7	7.0mmx5.0mm

Code	Stability
5	±25ppm
3	±50ppm

Code	Voltage
M	+1.8Vdc [2]
N	+2.5Vdc
L	+3.3Vdc

Code	Packing [3]
T	1k pcs./reel
R	3k pcs./reel

Code	Output
P	LVPECL
L	LVDS

Code	Temp. Range
C	-20°C to +70°C
I	-40°C to +85°C

Code	Frequency (MHz)[1]

Notes:

1) Frequency is recorded with 4 leading significant digits [includiing zeros] before and 5 significant digits [including zeroes] after the "M". [Ex. 1244.160000MHz = 1244M16000, 156.250000MHz =0156M25000, 608.750000MHz = 0608M75000]
2) LVDS output only.
3) Code T for package codes 5 and 7. Code T or R for package code 3 only.

Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.

Electrical Specifications

Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V_{CC}	-	-0.5	-	3.8	V
Supply Voltage	V_{CC}	±5%, LVDS only	1.71	1.8	1.89	V
		±10%	2.25	2.5	2.75	
			2.97	3.3	3.63	
Supply Current	I_{CC}	Maximum Load				mA
LVPECL		Maximum Current Value @ +3.3V	-	100	120	
LVDS			-	75	90	
Operating Temperature	T_A	-	-20	+25	+70	°C
			-40		+85	
Storage Temperature	T_{STG}	-	-55	-	+125	°C

Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range	f_O	-		100 - 2,100		MHz
Frequency Stability [Note 1]	$\Delta f/f_O$	-		25 or 50		±ppm
Aging	$\Delta f/f_{25}$	First Year @ +25°C, nominal V_{CC}	-3	-	3	ppm

1.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		LVPECL		-
Output Load	R_L	Terminated to V_{CC} - 2.0V	-	50	-	Ohms
Output Voltage Levels	V_{OH}	PECL Load	V_{CC} - 1.165	-	V_{CC} - 0.80	V
	V_{OL}		V_{CC} - 2.0	-	V_{CC} - 1.55	
Output Duty Cycle	SYM	@ V_{CC} - 1.3V	45	-	55	%
Differential Output Voltage	V_{OD}	R_L = 50 Ohms	595	-	930	mV
Rise and Fall Time	T_R, T_F	@ 20%/80% Levels, R_L = 50 Ohms	-	-	0.40	ns

Output Type	-	-		LVDS		-
Output Load	R_L	Between Outputs	-	100	-	Ohms
Output Voltage Levels	V_{OH}	LVDS Load	-	1.40	1.60	V
	V_{OL}		0.90	1.10	-	
Output Duty Cycle	SYM	@ 1.25V	45	-	55	%
Differential Output Voltage	V_{OD}	R_L = 100 Ohms	250	-	450	mV
Offset Voltage	V_{OS}	LVDS Load	1.20	1.25	1.30	V
Rise and Fall Time	T_R, T_F	@ 20%/80% Levels, R_L = 100 Ohms	-	-	0.40	ns

Electrical Specifications

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Start Up Time	T_S	Application of V_{CC}	-	5	10	ms
Enable Function [Tri-State]						
Enable Input Voltage	V_{IH}	Pin 1 Logic '1', Output Enabled	$0.8V_{CC}$	-	-	V
Disable Input Voltage	V_{IL}	Pin 1 Logic '0', Output Disabled	-	-	$0.2V_{CC}$	V
Disable Current	I_{IL}	Pin 1 Logic '0', Output Disabled, LVPECL	-	99	-	mA
		Pin 1 Logic '0', Output Disabled, LVDS	-	74	-	
Disable Time	T_{PLZ}	Pin 1 Logic '0', Output Disabled	-	-	10	µs
Enable Time	T_{PLZ}	Pin 1 Logic '1', Output Enabled	-	-	2.5	ms
Phase Jitter, RMS	tjrms	Bandwidth 12 kHz - 20 MHz	-	150	300	fs

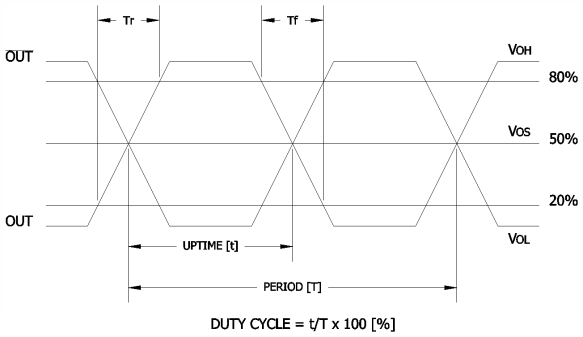
Enable Truth Table

LVPECL or LVDS

Pin 1	Pin 4 & Pin 5
Logic '1'	Output Enabled
Open	Output Enabled
Logic '0'	Output Disabled, High Impedance

Output Waveform

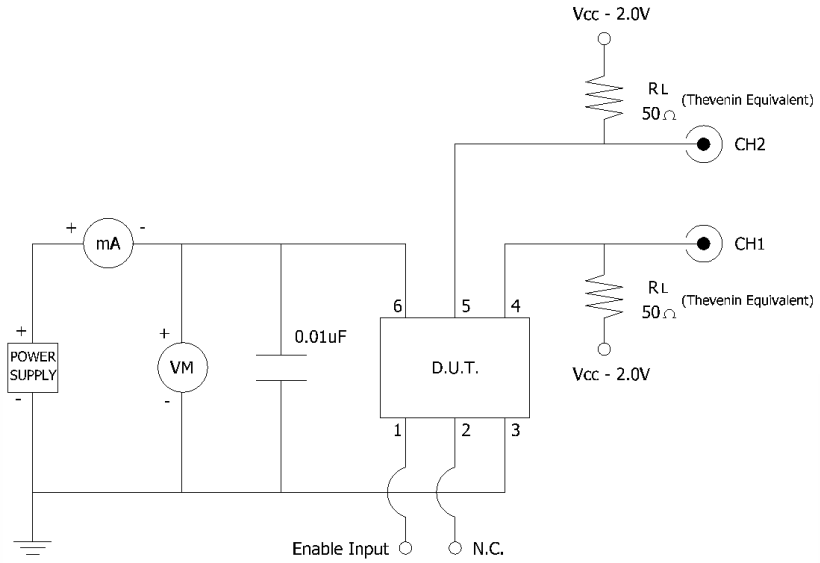
LVPECL or LVDS



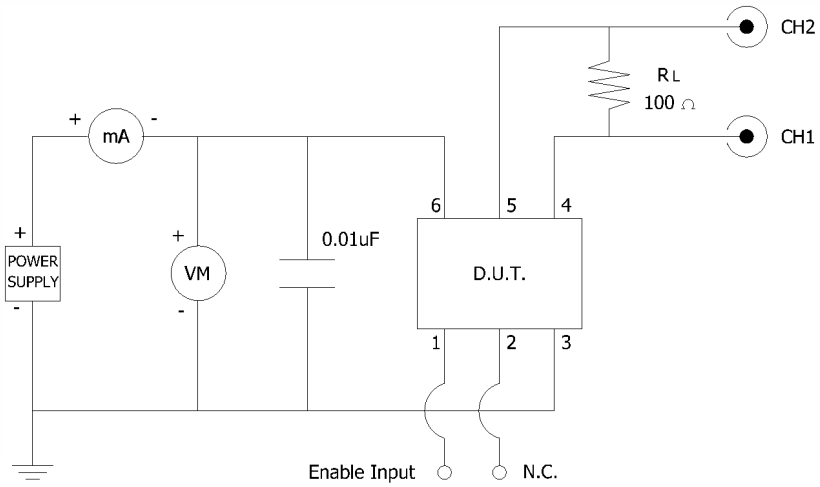
Electrical Specifications

Test Circuit

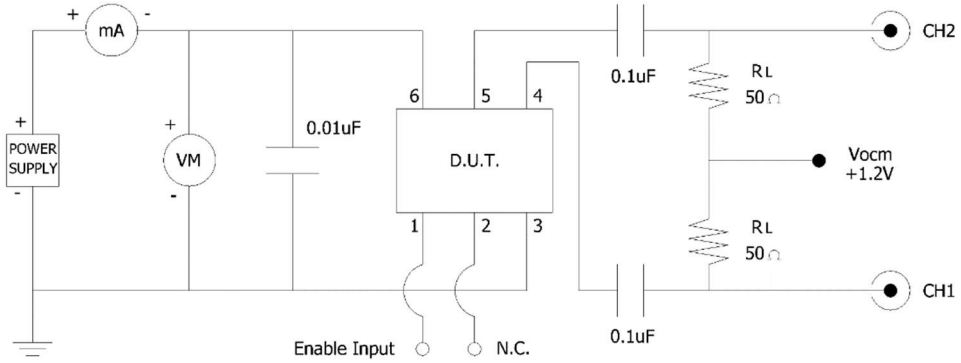
LVPECL



LVDS



LVDS @ +1.8V

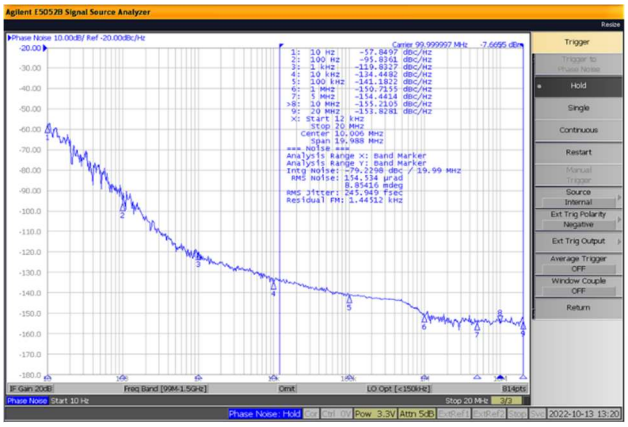


Electrical Specifications

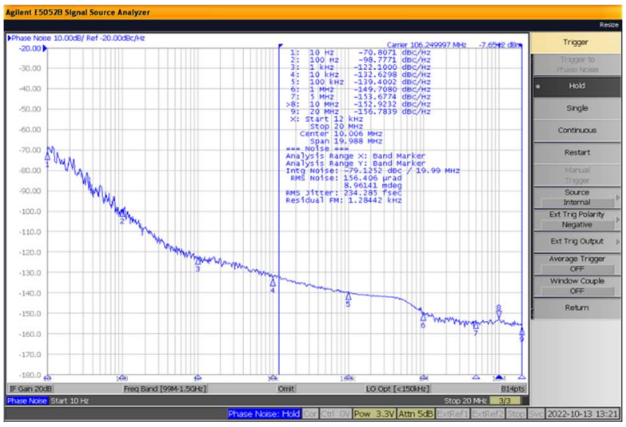
Performance Data

Phase Noise [typical]

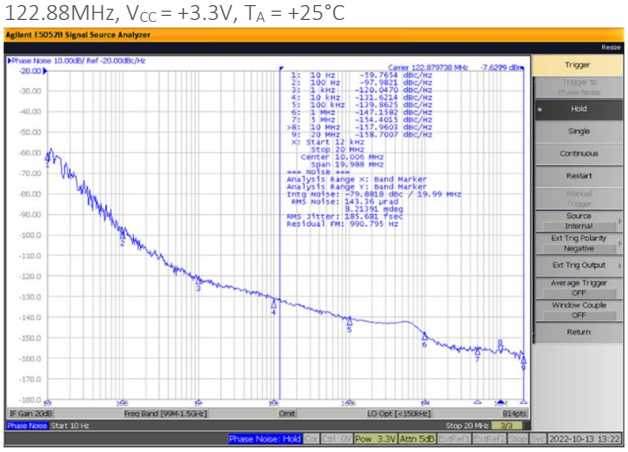
100MHz, V_{CC} = +3.3V, T_A = +25°C



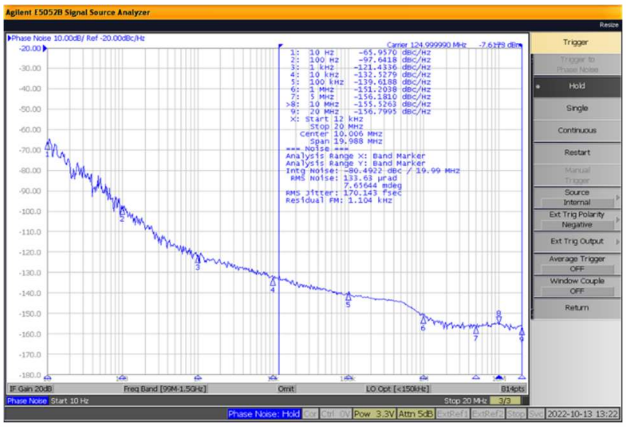
106.25MHz, V_{CC} = +3.3V, T_A = +25°C



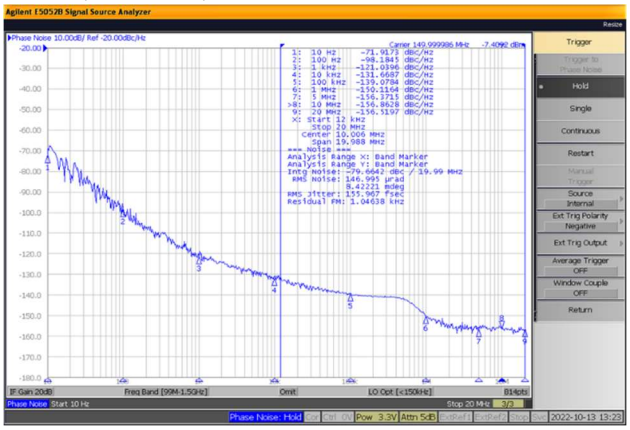
122.88MHz, V_{CC} = +3.3V, T_A = +25°C



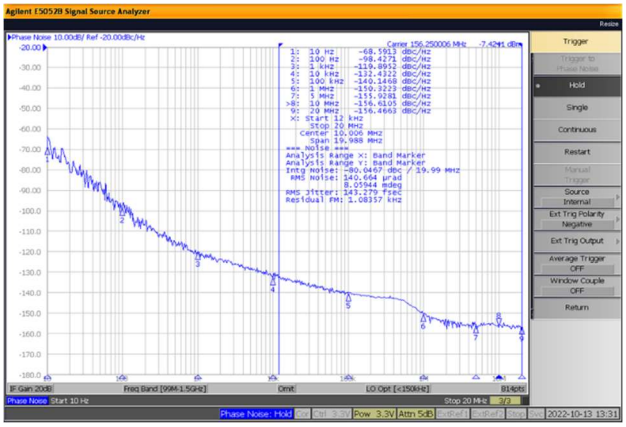
125MHz, V_{CC} = +3.3V, T_A = +25°C



150MHz, V_{CC} = +3.3V, T_A = +25°C



156.25MHz, V_{CC} = +3.3V, T_A = +25°C

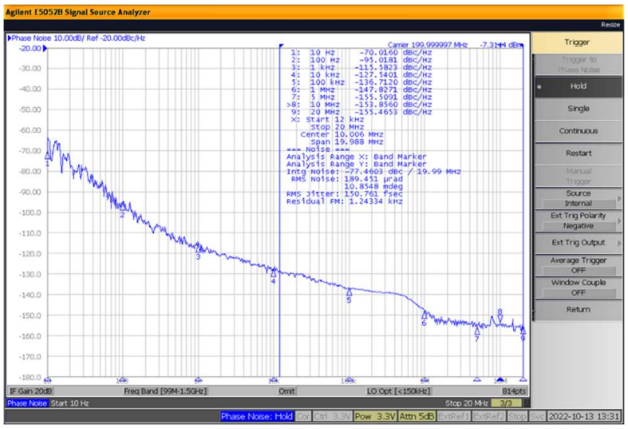


Electrical Specifications

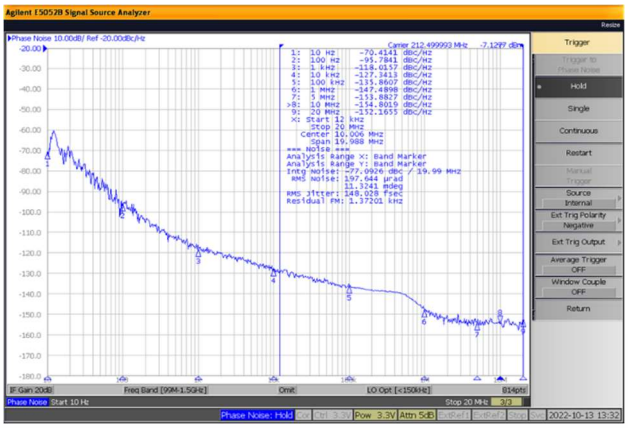
Performance Data

Phase Noise [typical]

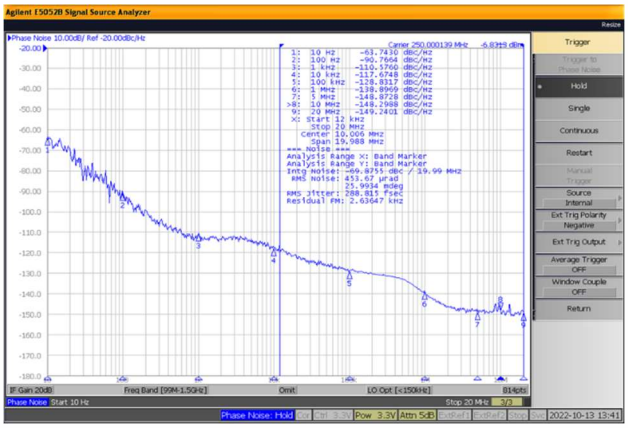
200MHz, V_{CC} = +3.3V, T_A = +25°C



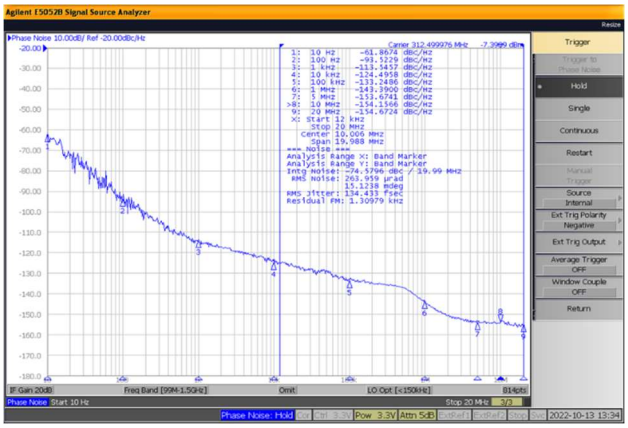
212.5MHz, V_{CC} = +3.3V, T_A = +25°C



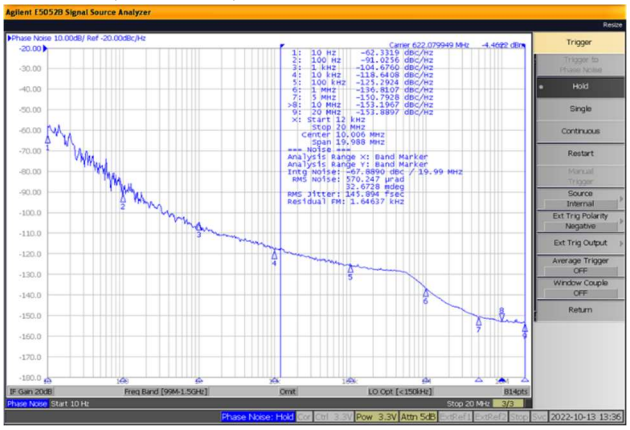
250MHz, V_{CC} = +3.3V, T_A = +25°C



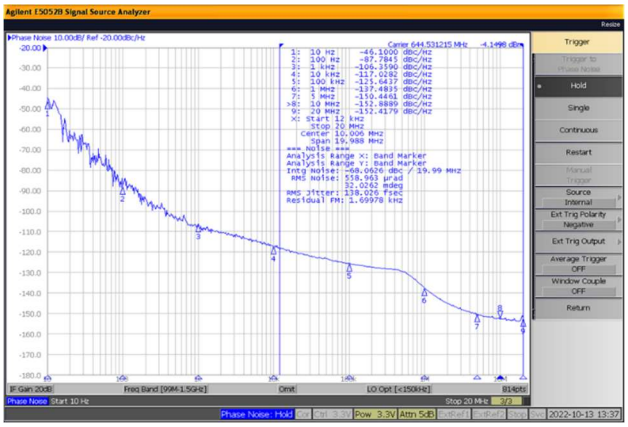
312.5MHz, V_{CC} = +3.3V, T_A = +25°C



622.08MHz, V_{CC} = +3.3V, T_A = +25°C



644.53125MHz, V_{CC} = +3.3V, T_A = +25°C



Electrical Specifications

Performance Data

Phase Noise Tabulated

Typical, V_{CC} = +3.3V, T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
100.0000MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-57.8497	
		@ 100Hz	-95.8361	
		@ 1kHz	-119.8327	
	-	@ 10kHz	-134.4482	dBc/Hz
		@ 100kHz	-141.1822	
		@ 1MHz	-150.7155	
		@ 5MHz	-154.4414	
		@ 10MHz	-155.2105	
		@ 20MHz	-153.8281	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	245.9490	fs

Typical, V_{CC} = +3.3V, T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
106.250MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-70.8071	
		@ 100Hz	-98.7771	
		@ 1kHz	-122.1000	
	-	@ 10kHz	-132.6298	dBc/Hz
		@ 100kHz	-139.4002	
		@ 1MHz	-149.7080	
		@ 5MHz	-153.6774	
		@ 10MHz	-152.9232	
		@ 20MHz	-156.7839	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	234.2850	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
122.8800MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-59.7654	
		@ 100Hz	-97.9821	
		@ 1kHz	-120.0470	
	-	@ 10kHz	-131.6214	dBc/Hz
		@ 100kHz	-139.8625	
		@ 1MHz	-147.1582	
		@ 5MHz	-154.4015	
		@ 10MHz	-157.9603	
		@ 20MHz	-158.7007	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	185.6810	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
125.0000MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-65.9570	
		@ 100Hz	-97.6418	
		@ 1kHz	-121.4336	
	-	@ 10kHz	-132.5279	dBc/Hz
		@ 100kHz	-139.6188	
		@ 1MHz	-151.2038	
		@ 5MHz	-156.1810	
		@ 10MHz	-155.5263	
		@ 20MHz	-156.7995	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	170.1430	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
150.0000MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-71.9173	
		@ 100Hz	-98.1845	
		@ 1kHz	-121.0396	
	-	@ 10kHz	-131.6687	dBc/Hz
		@ 100kHz	-139.0784	
		@ 1MHz	-150.1164	
		@ 5MHz	-156.3715	
		@ 10MHz	-156.8628	
		@ 20MHz	-156.5197	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	155.9670	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
156.2500MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-68.5913	
		@ 100Hz	-98.4271	
		@ 1kHz	-119.8952	
	-	@ 10kHz	-132.4322	dBc/Hz
		@ 100kHz	-140.1468	
		@ 1MHz	-150.3223	
		@ 5MHz	-155.9281	
		@ 10MHz	-156.6105	
		@ 20MHz	-156.4663	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	143.2790	fs

Electrical Specifications

Performance Data

Phase Noise Tabulated

Typical, V_{CC} = +3.3V, T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
200.0000MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-70.0160	
		@ 100Hz	-95.0181	
		@ 1kHz	-115.5823	
	-	@ 10kHz	-127.5401	dBc/Hz
		@ 100kHz	-136.7120	
		@ 1MHz	-147.8271	
		@ 5MHz	-155.5091	
		@ 10MHz	-153.8560	
		@ 20MHz	-155.4653	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	150.7610	fs

Typical, V_{CC} = +3.3V, T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
212.5000MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-70.4141	
		@ 100Hz	-95.7841	
		@ 1kHz	-118.0157	
	-	@ 10kHz	-127.3413	dBc/Hz
		@ 100kHz	-135.8607	
		@ 1MHz	-147.4898	
		@ 5MHz	-153.8827	
		@ 10MHz	-154.8019	
		@ 20MHz	-152.1655	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	148.0280	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
250.0000MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-63.7430	
		@ 100Hz	-90.7664	
		@ 1kHz	-110.5760	
	-	@ 10kHz	-117.6748	dBc/Hz
		@ 100kHz	-128.8317	
		@ 1MHz	-138.8969	
		@ 5MHz	-148.8728	
		@ 10MHz	-148.2933	
		@ 20MHz	-149.2401	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	288.8150	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
312.5000MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-61.8674	
		@ 100Hz	-93.5229	
		@ 1kHz	-113.5457	
	-	@ 10kHz	-124.4958	dBc/Hz
		@ 100kHz	-133.2486	
		@ 1MHz	-143.3900	
		@ 5MHz	-153.6741	
		@ 10MHz	-154.1566	
		@ 20MHz	-154.6724	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	134.4330	fs

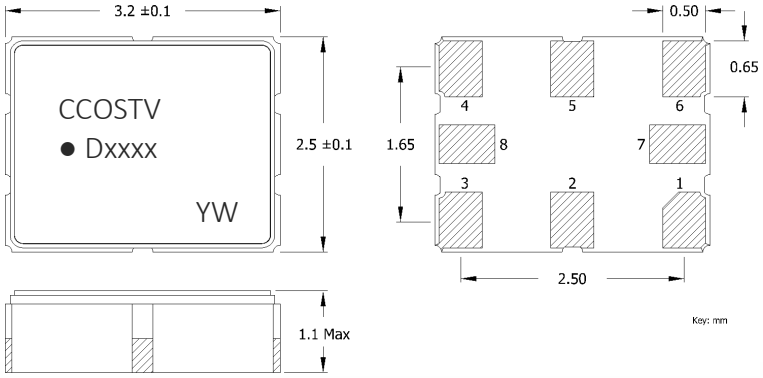
PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
622.0800MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-62.3319	
		@ 100Hz	-91.0256	
		@ 1kHz	-104.6760	
	-	@ 10kHz	-118.6408	dBc/Hz
		@ 100kHz	-125.2924	
		@ 1MHz	-136.8107	
		@ 5MHz	-150.7928	
		@ 10MHz	-153.1967	
		@ 20MHz	-153.8897	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	145.8940	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
644.53125MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-46.1000	
		@ 100Hz	-87.7845	
		@ 1kHz	-106.3590	
	-	@ 10kHz	-117.0282	dBc/Hz
		@ 100kHz	-125.6437	
		@ 1MHz	-137.4835	
		@ 5MHz	-150.4461	
		@ 10MHz	-152.8889	
		@ 20MHz	-152.4179	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	138.0260	fs

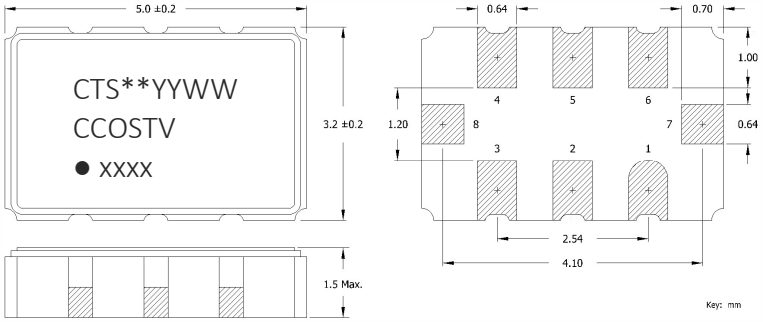
Mechanical Specifications

Package Drawing

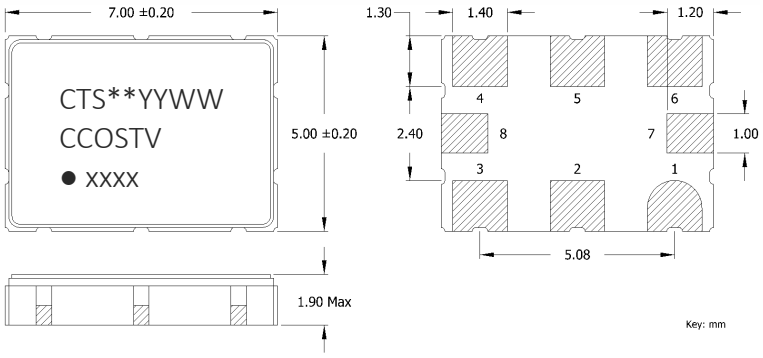
CC3



CC5



CC7



Marking Information

CC3

1. CC – Model series.
2. O – Output Type; P = LVPECL, L = LVDS.
3. ST – Frequency Stability/Temperature Code.
   [Refer to Ordering Information]
4. V – Voltage Code; M = 1.8V, N = 2.5V, L = 3.3V.
5. D – Date Code. See Table I for codes.
6. xxxx – Frequency Code.
   3-digits, frequencies below 100MHz
   4-digits, frequencies 100MHz or greater
   [See document 016-1454-0, Frequency Code Tables.]
7. YW [Optional] – CTS Internal Marking for Traceability.

CC5 and CC7

1. ** - Manufacturing Site Code.
2. YYWW – Date Code; YY – year, WW – week.
3. CC – Model series.
4. O – Output Type; P = LVPECL, L = LVDS.
5. ST – Frequency Stability/Temperature Code.
   [Refer to Ordering Information]
6. V – Voltage Code; M = 1.8V, N = 2.5V, L = 3.3V.
7. xxxx – Frequency Code.
   3-digits, frequencies below 100MHz
   4-digits, frequencies 100MHz or greater
   [See document 016-1454-0, Frequency Code Tables.]

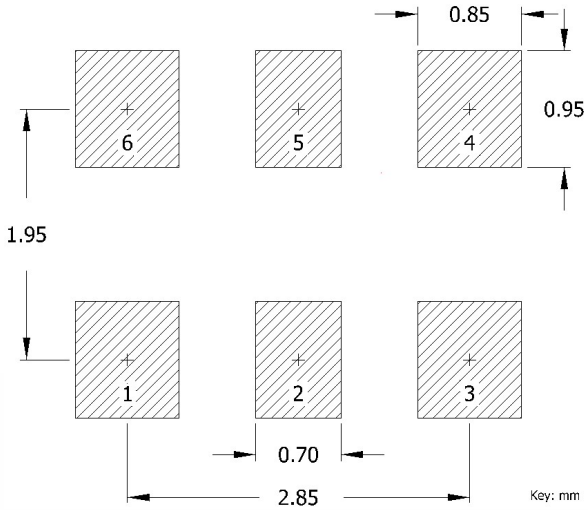
Notes

1. JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
2. Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
3. MSL = 1.

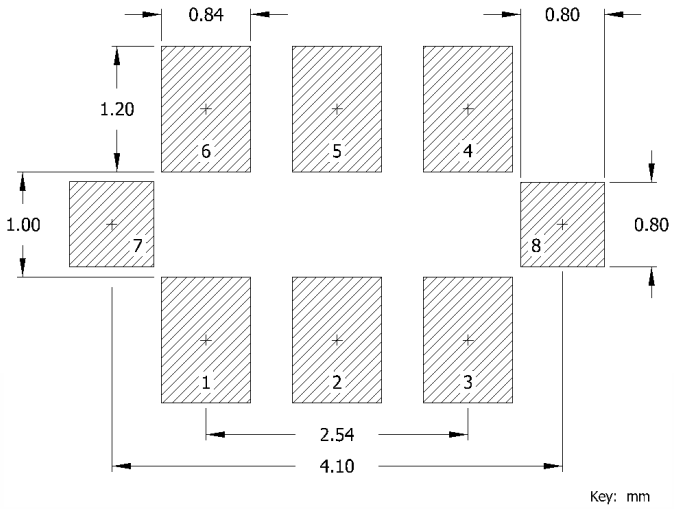
Mechanical Specifications

Recommended Pad Layout

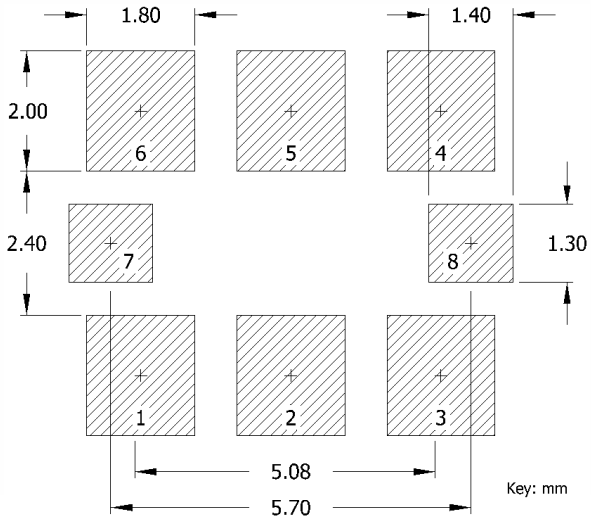
CC3



CC5



CC7



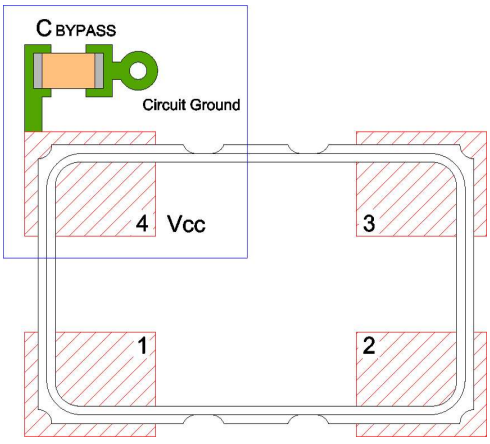
Pin Assignments

LVPECL or LVDS

Pin	Symbol	Function
1	EOH	Enable
2	N.C.	No Connect
3	GND	Circuit & Package Ground
4	Output	RF Output
5	$\overline{\text{Output}}$	Complimentary RF Output
6	V_{CC}	Supply Voltage
7	N.C.	Do Not Connect
8	N.C.	Do Not Connect

VOLTAGE SUPPLY - BYPASS CAPACITOR

Proper filtering of high frequency noise riding on the voltage supply line is critical to eliminating the injecting of that noise into the oscillator and throughout the system. It is recommended that a 0.1µF [100nF] capacitor be inserted from the Vcc pin to circuit ground. The bypass capacitor placement should be as close to the Vcc pad as possible with a short trace routing to circuit ground.



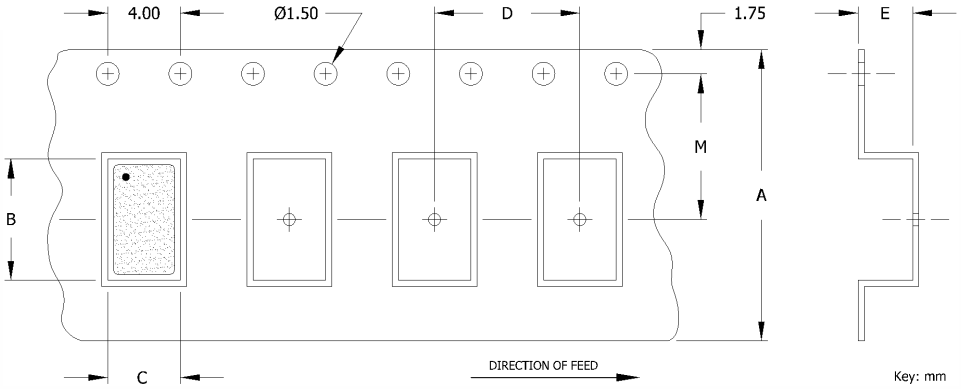
Mechanical Specifications

Table I - Date Code, Beginning year 2021

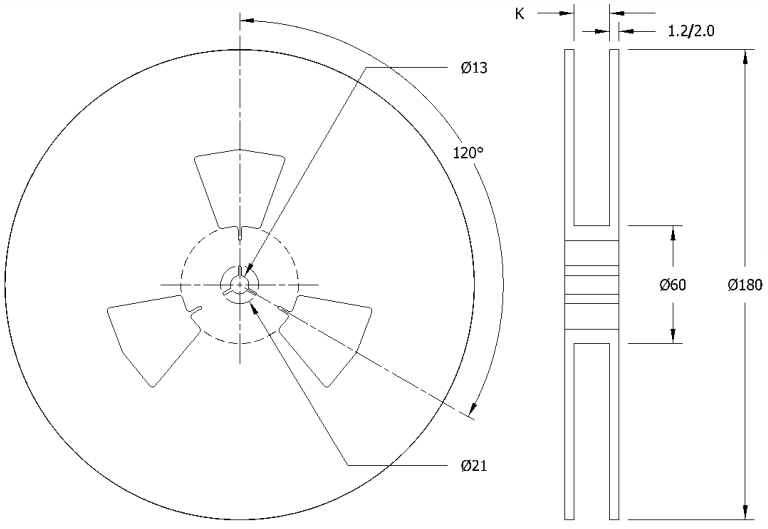
YEAR \ MONTH	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
2021 2025 2029 2033 2037	A	B	C	D	E	F	G	H	J	K	L	M
2022 2026 2030 2034 2038	N	P	Q	R	S	T	U	V	W	X	Y	Z
2023 2027 2031 2035 2039	a	b	c	d	e	f	g	h	j	k	l	m
2024 2028 2032 2036 2040	n	p	q	r	s	t	u	v	w	x	y	z

Packaging - Tape and Reel

Tape Drawing



Reel Drawing



Tape Dimensions

PACKAGE	A	B	C	D	E	M	QUANTITY
CC3	8.00	3.40	2.70	4.00	1.40	3.50	3000
CC5	12.00	5.30	3.60	8.00	1.40	5.50	1000
CC7	16.00	7.30	5.30	8.00	1.90	7.50	1000

Reel Dimensions

K
8.00
13.00
17.20

Notes

1. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.